ADCS OF SDR

PARAMETERS, DESIGN CONSIDERATIONS AND IMPLEMENTATIONS

Presented by Spectrum Signal Processing and Intersil Corporation

August 2011

Company Overview

Intersil

Headquarters: Milpitas, CA

Solutions: Best-in-class solutions for video processing, active cables, and high-speed/high resolution ADCs. Intersil strives to provide products that offer Simplicity, Innovation, & Intelligence to their customers.

Spectrum Signal Processing by Vecima

Headquarters: Burnaby, BC

Solutions: High-performance data acquisition (RF, analog and digital I/O) and reconfigurable signal and video processing hardware and systems for ISR (SIGINT, COMINT, ELINT), SDR, MILCOM and SATCOM markets. Spectrum is part of Vecima Networks Inc.

Presenters

Mark Rives, Principal Applications Engineer at Intersil
Mark is a Principal Applications Engineer at Intersil where he supports high speed data converter customers and participates in new product definition.

Edward Kohler, Strategic Marketing Manager at Intersil
Edward is Intersil's Strategic Marketing Manager for high speed data converters and ADC drivers.

Tudor Davies, Director of Technology at Spectrum
Tudor is the Director of Technology at Spectrum, and in this role, he defines the architecture of Spectrum's future products and projects.

Outline

Software Defined Radio (SDR) Overview

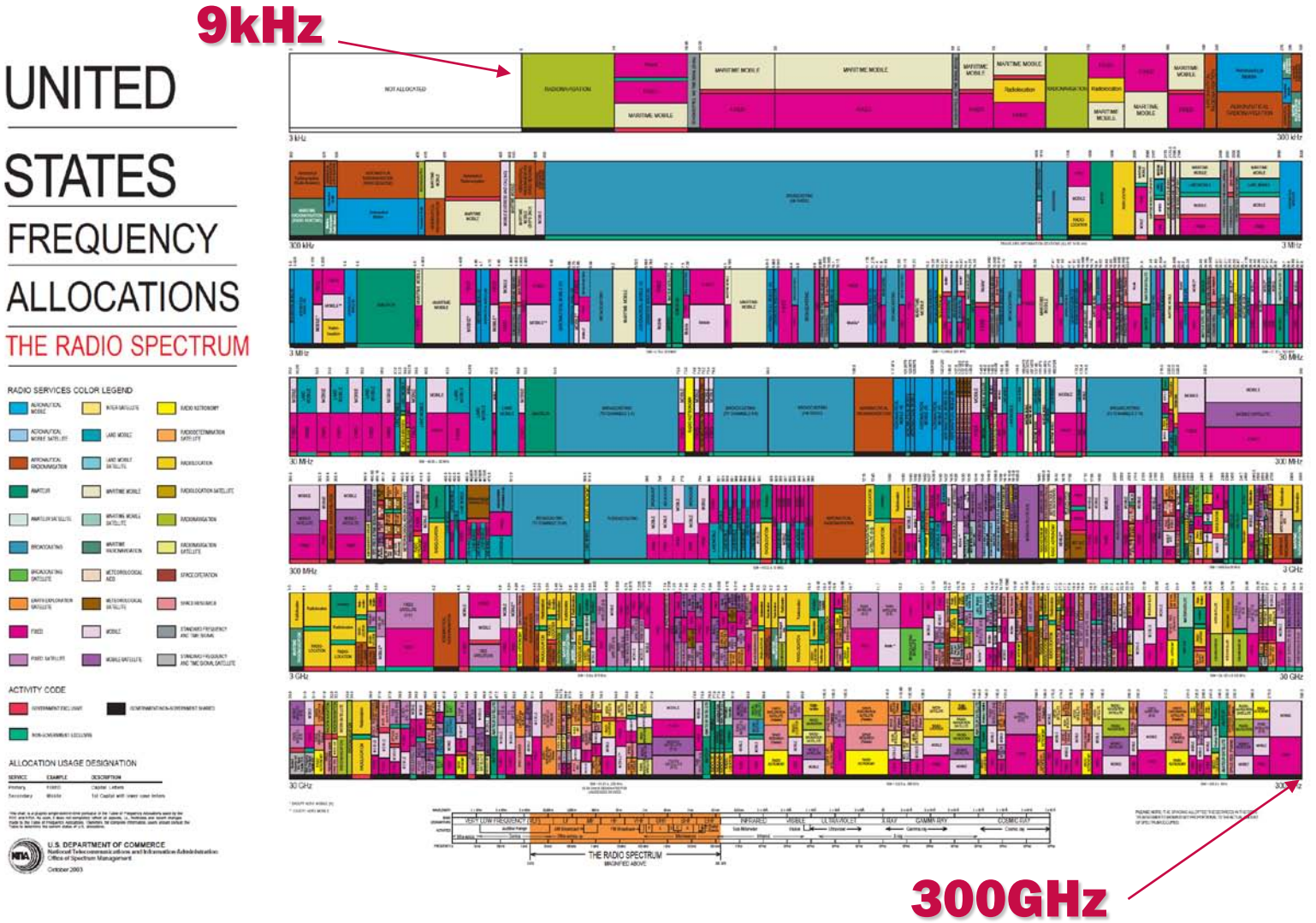
ADC Fundamentals and Specifications

How ADC Specifications Impact SDR

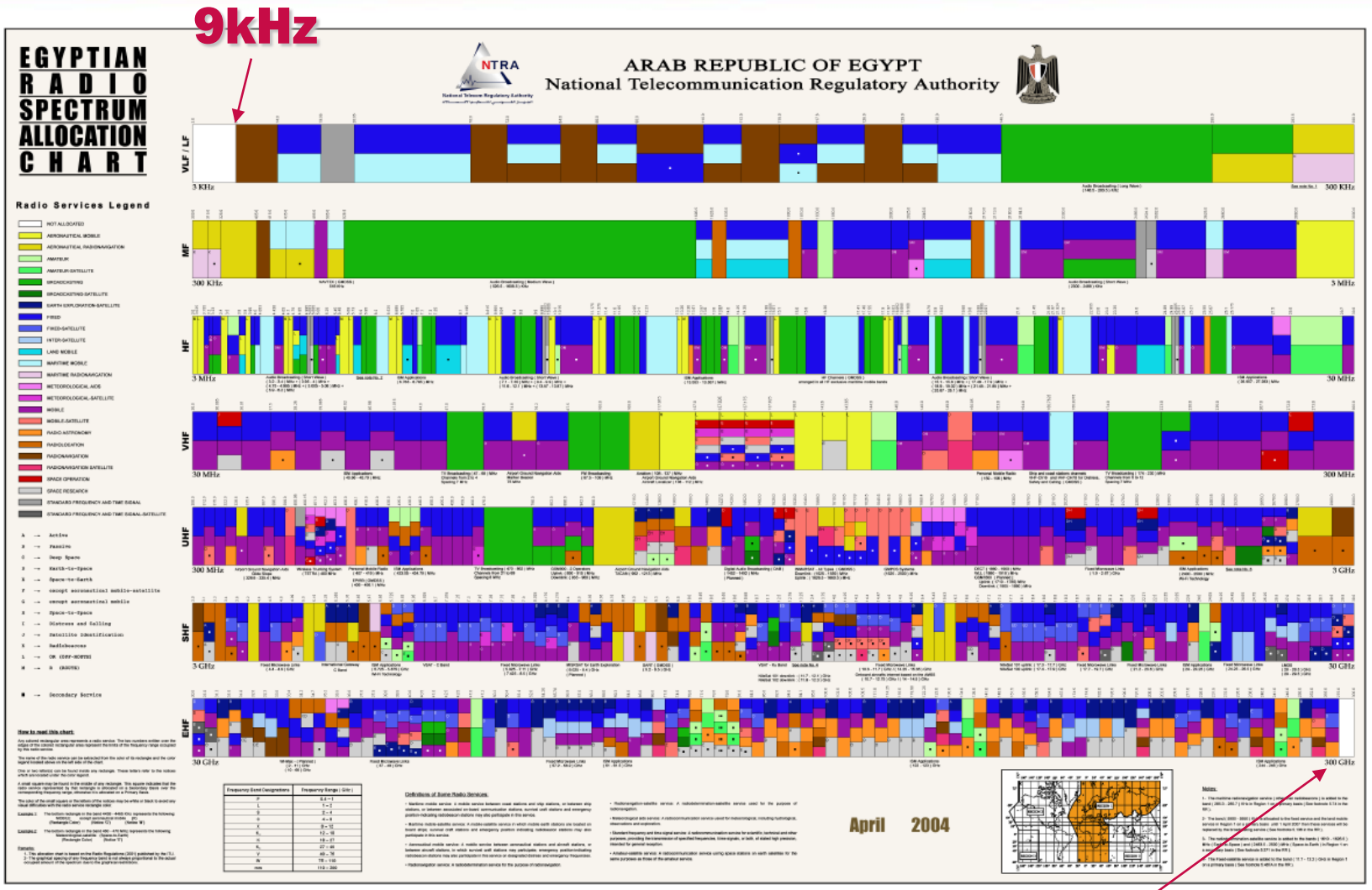
Small Form-Factor Real World Implementation

Summary

The United States RF Spectrum

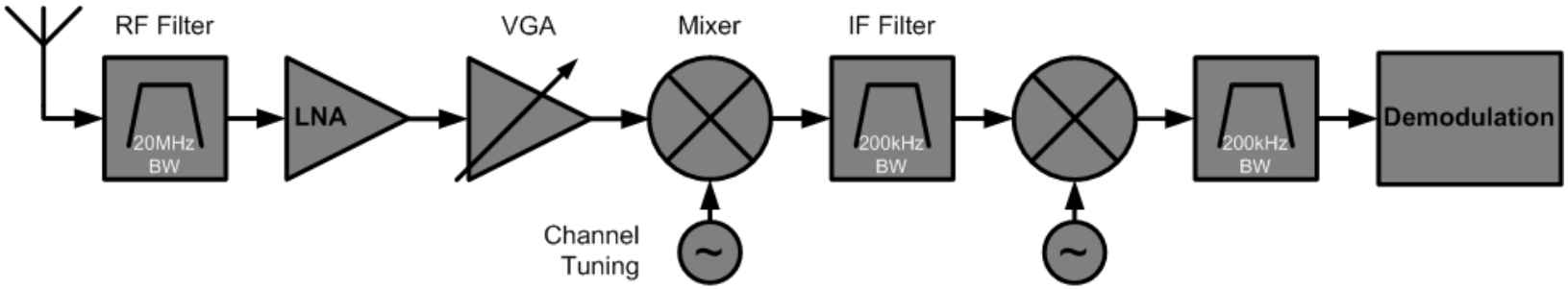


The RF Spectrum in Egypt

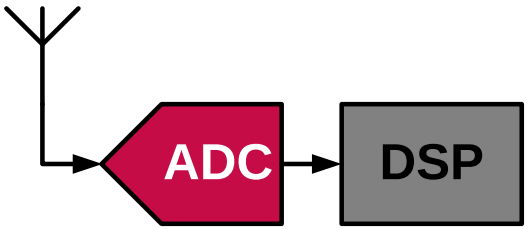


SDR Overview

Traditional receivers only cover a single channel in a limited number of bands because they are made with dedicated hardware for a specific signal or waveform.



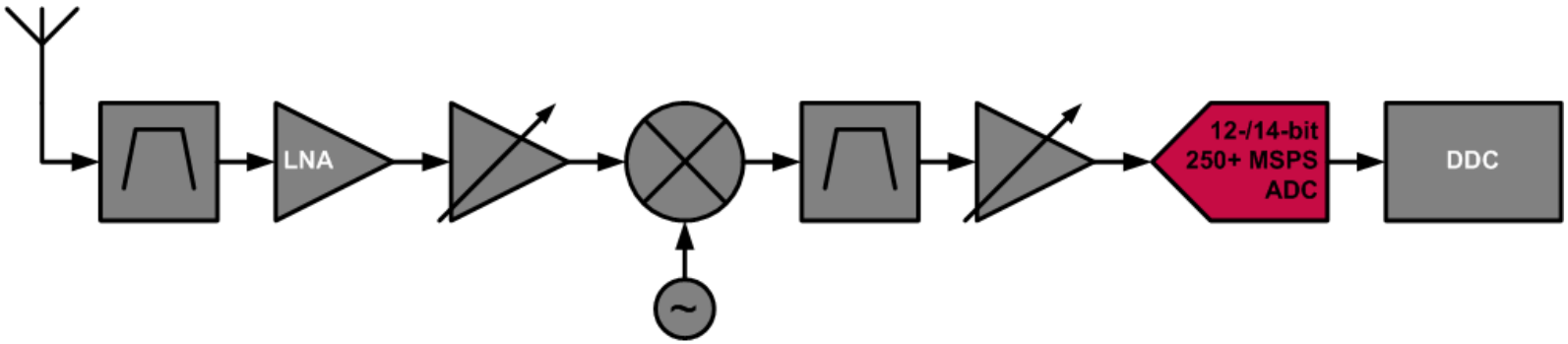
A Software Defined Radio (SDR) is a radio where digitizing the signal allows circuitry previously implemented in dedicated hardware to be moved into the digital domain.



Ideally, an ADC could directly sample the signal from the antenna.

SDR Overview (continued)

ADCs do not have infinite dynamic range or infinite input bandwidth so additional components are still required to condition the ADC input signal.



After the signal is digitized, software can control the channel frequency, bandwidth and modulation format.

Placing the ADC as close to the antenna as possible provides the most flexibility but must be traded off against performance limitations.

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ADC Fundamentals

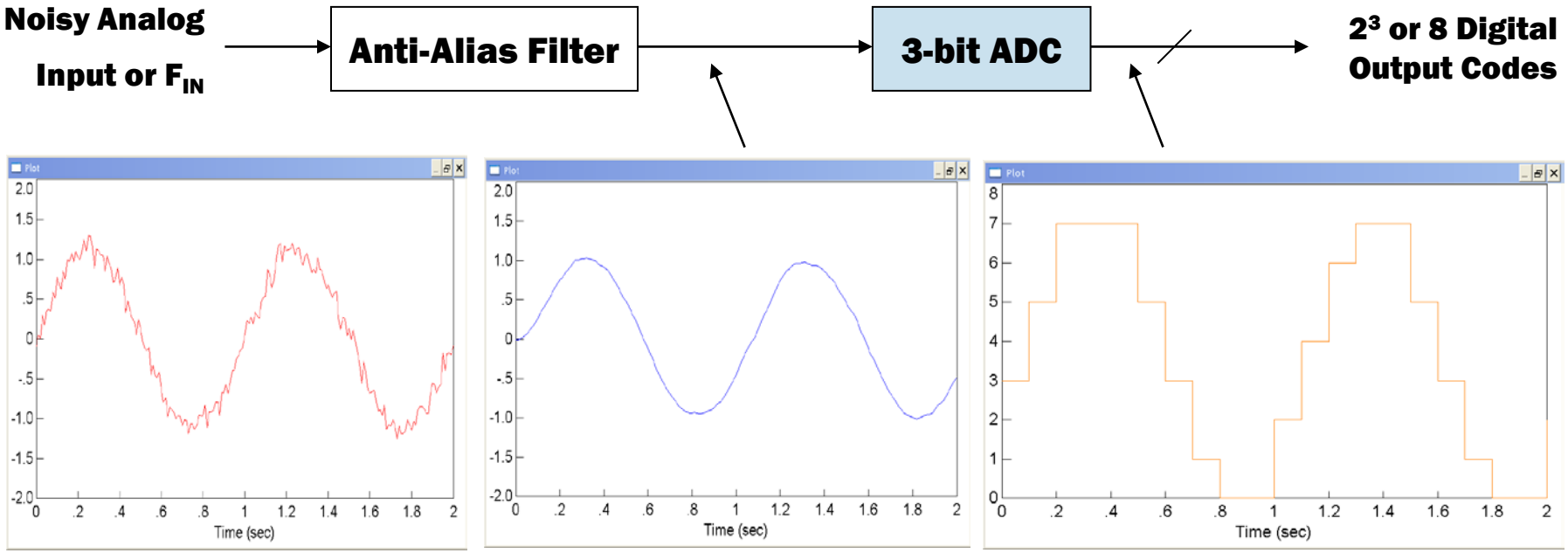
ADC = Analog to Digital Converter

The ADC clock (F_{SAMPLE} or F_S) sets the sample interval

The sampling process introduces side effects

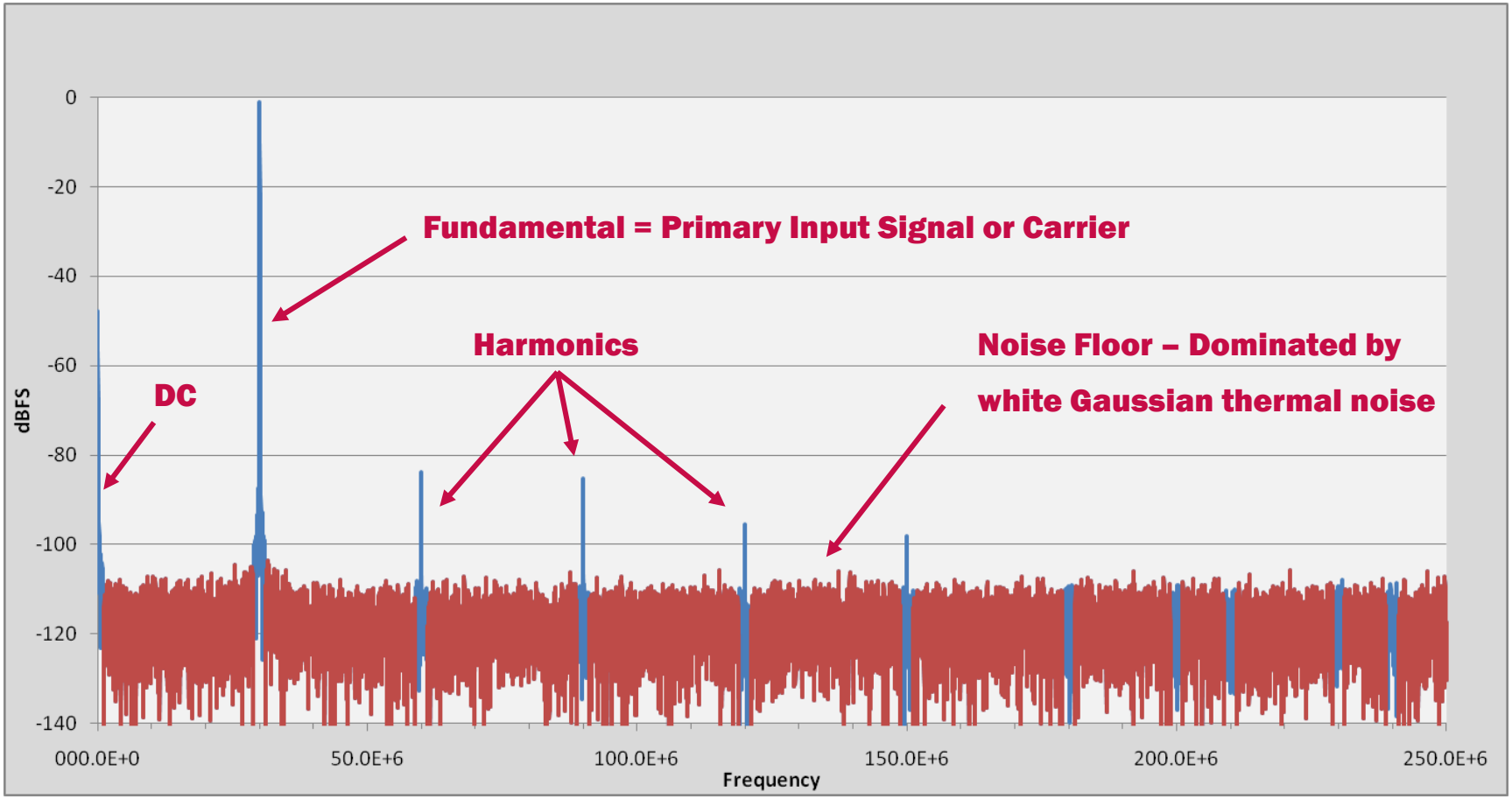
Performance of the sampling process is specified by

- Noise – SNR
- Distortion – SFDR, THD, INL



Signal to Noise Ratio (SNR)

SNR = the sum of all power except DC, fundamental and the first ten harmonics relative to full-scale power (dBFS) or to signal power (dBc)



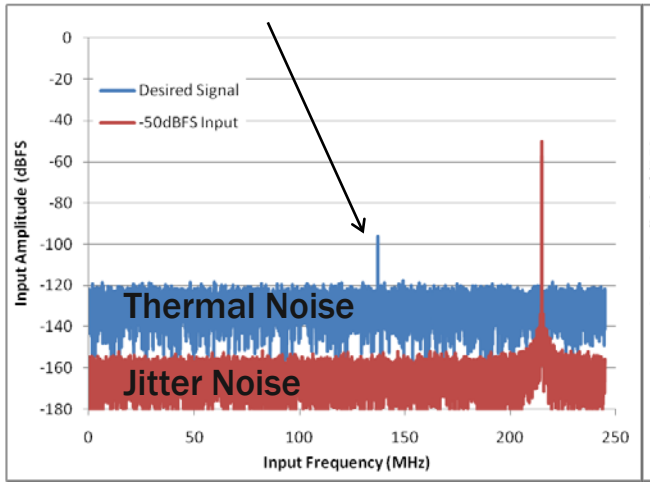
Clock Jitter Reduces SNR

Clock uncertainty -> Sample time uncertainty

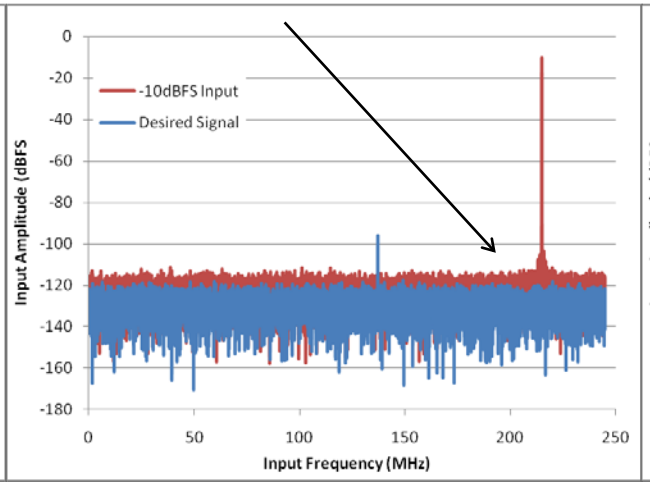
Result: Output voltage errors

- The SNR may be dominated by thermal noise or jitter noise
- The jitter noise is constant relative to the input amplitude
- A very large signal may cause a small signal to be lost in the noise
- Lower clock jitter can offer higher sensitivity

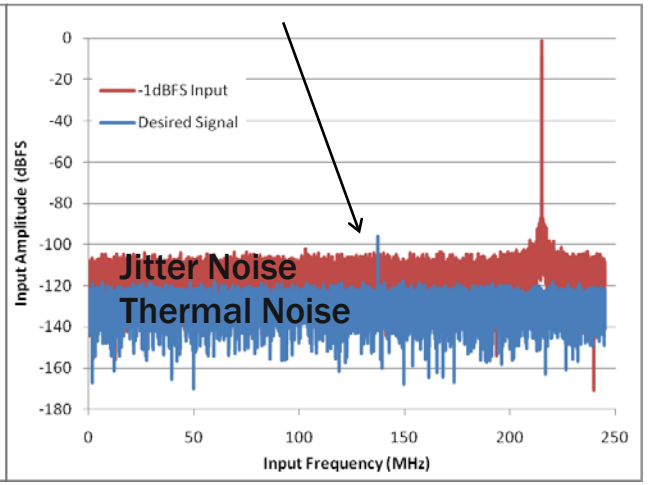
Desired signal, constant amplitude



Large signal with jitter raises the noise floor

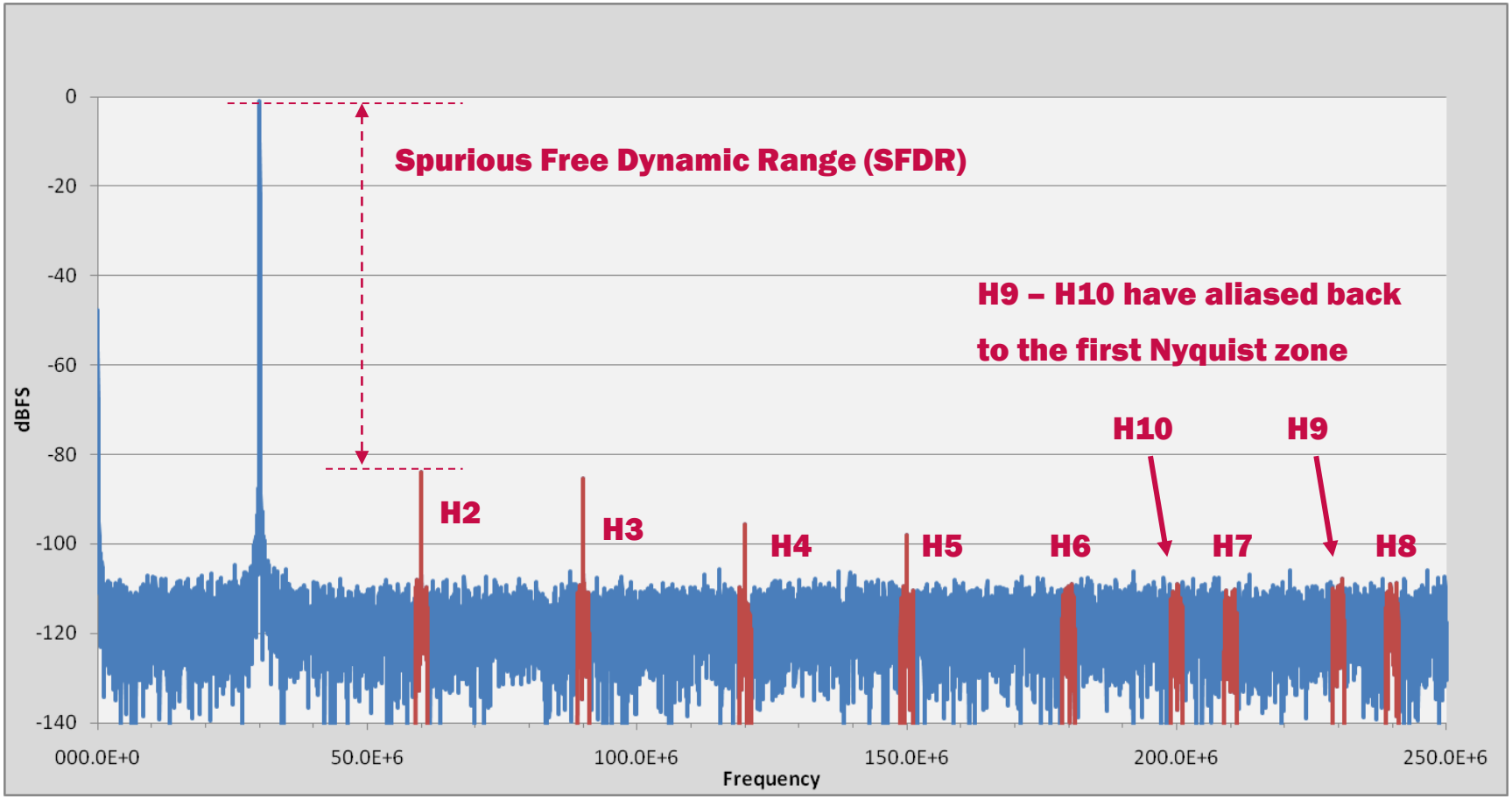


Jitter noise masks the desired signal

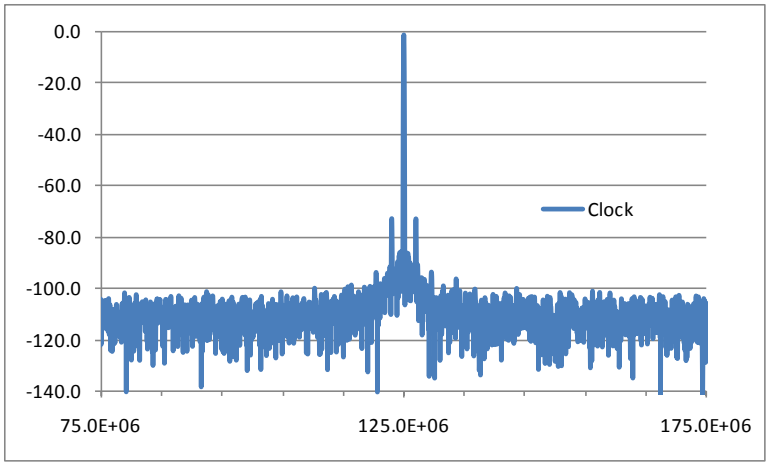


Distortion (THD, SFDR)

THD = Total Harmonic Distortion is the sum of power in the first ten harmonics relative to the fundamental signal power (dBc)

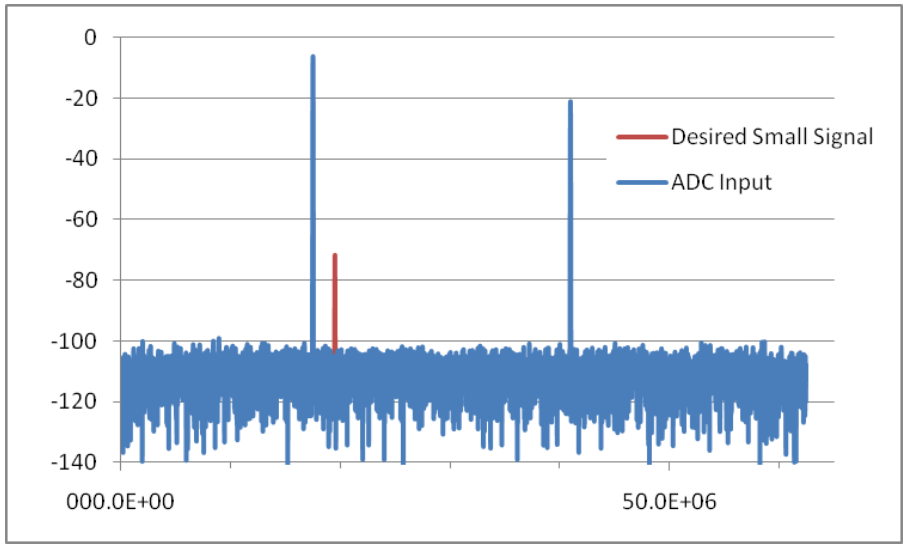


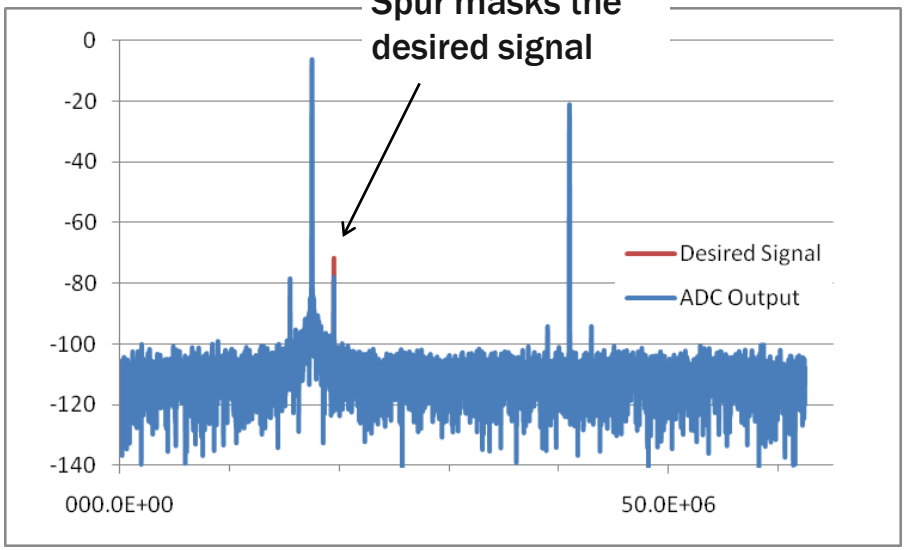
Clock Spurs



Any signal on the ADC's clock input will be convolved (mixed) with the analog input

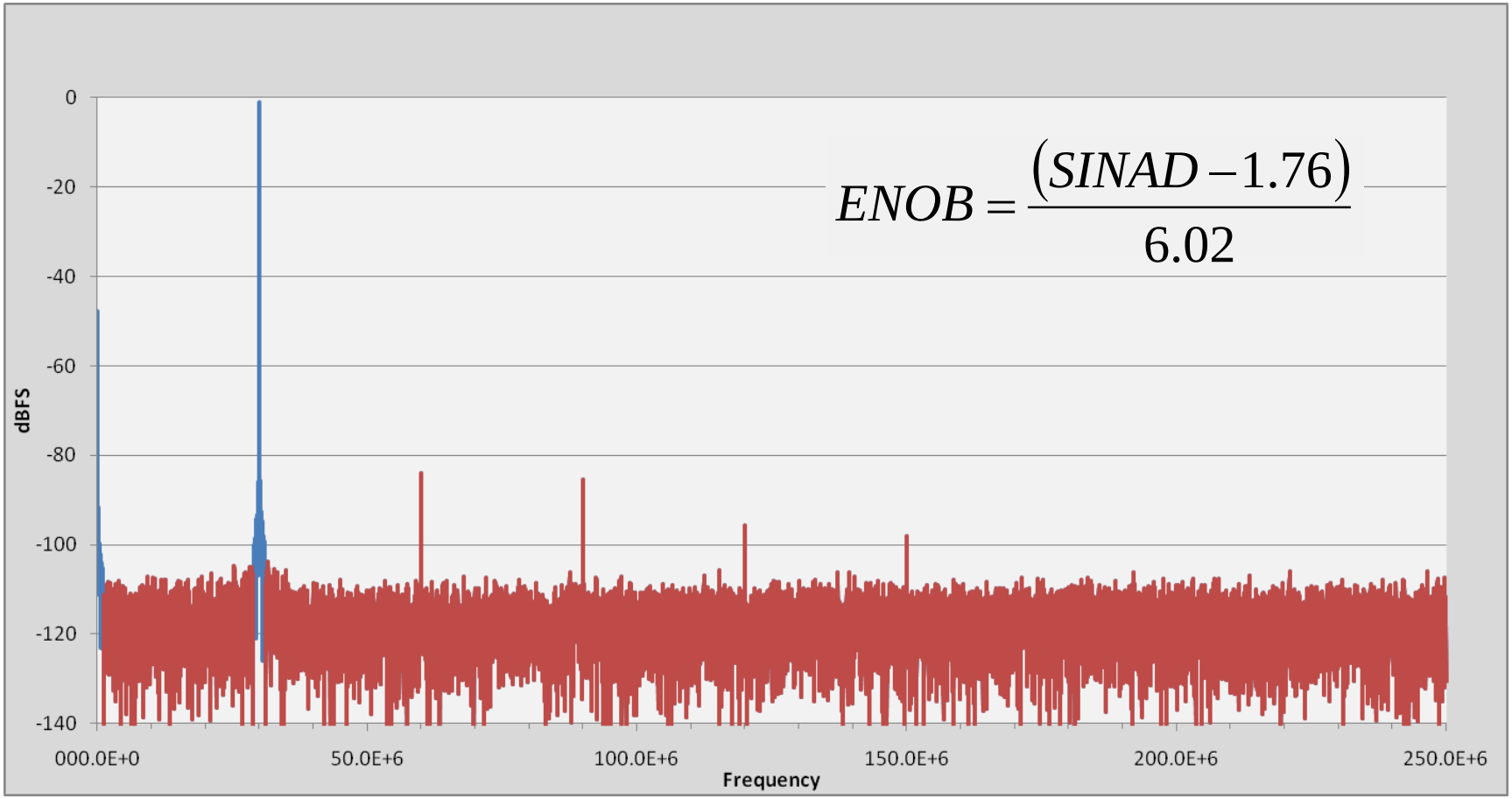
- Any spurs or non-harmonic content on the clock signal will appear around every analog input signal and may mask a desired signal





Noise + Distortion Specifications

SINAD = the sum of all power except DC and the fundamental relative to the signal power (dBc)

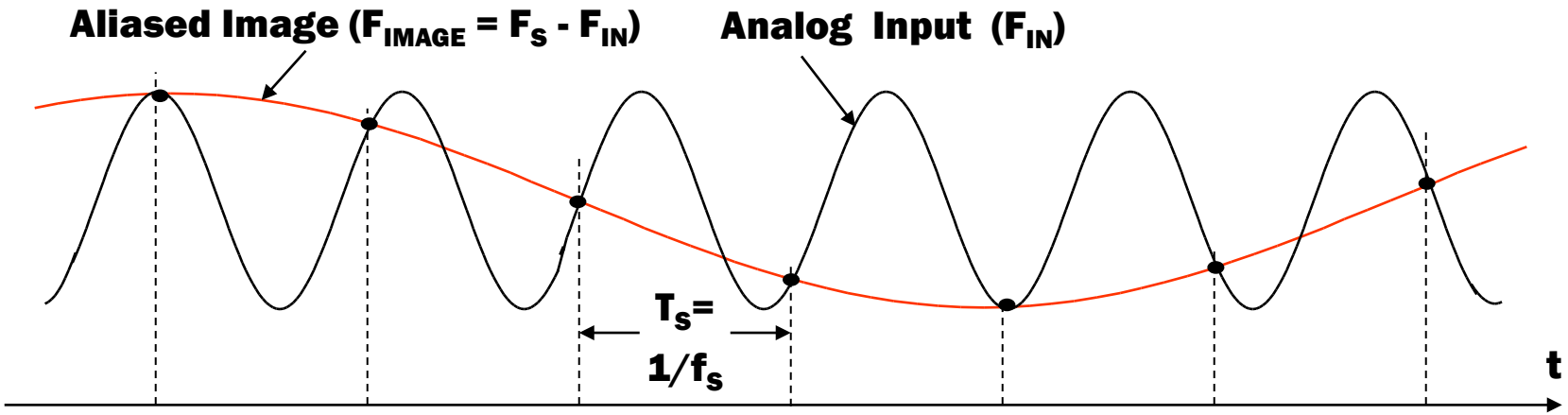


Aliasing

All signals sampled by the ADC will be output in the first Nyquist zone (DC to Fs/2) therefore,

If there are any unwanted signals (including noise) above Fs/2 they must be filtered prior to sampling

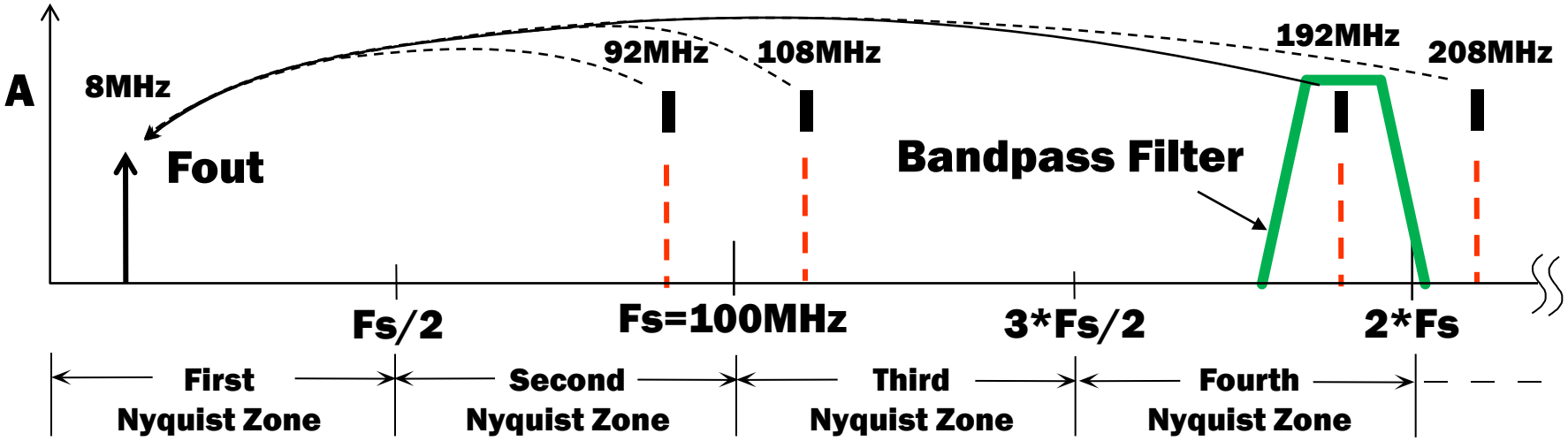
- Unwanted signals above Fs/2 can interfere with desired signals
- Once sampled, the unwanted signals cannot be removed
- The Analog Input (F_{IN}) and Aliased Image (F_{IMAGE}) are identical at the ADC output



Sub-Sampling

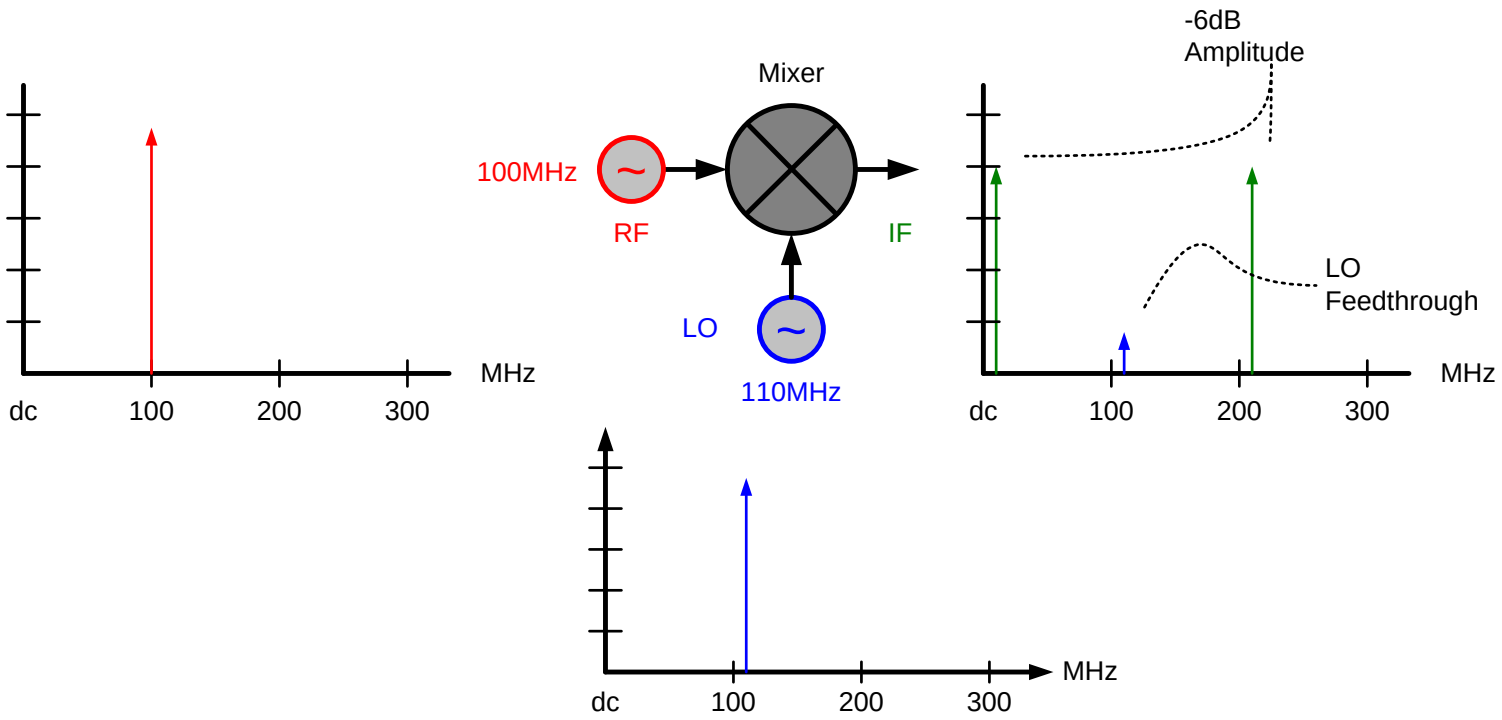
We can take advantage of aliasing to sample narrow-band signals beyond the first Nyquist zone

- All the images will appear in the first Nyquist zone at the ADC output
- Filtering must be used to select the desired image
- Commonly used for Intermediate Frequency (IF) sampling receivers
- A wide ADC input bandwidth enables high-IF sub-sampling
- The signal of interest must fit within a single Nyquist zone

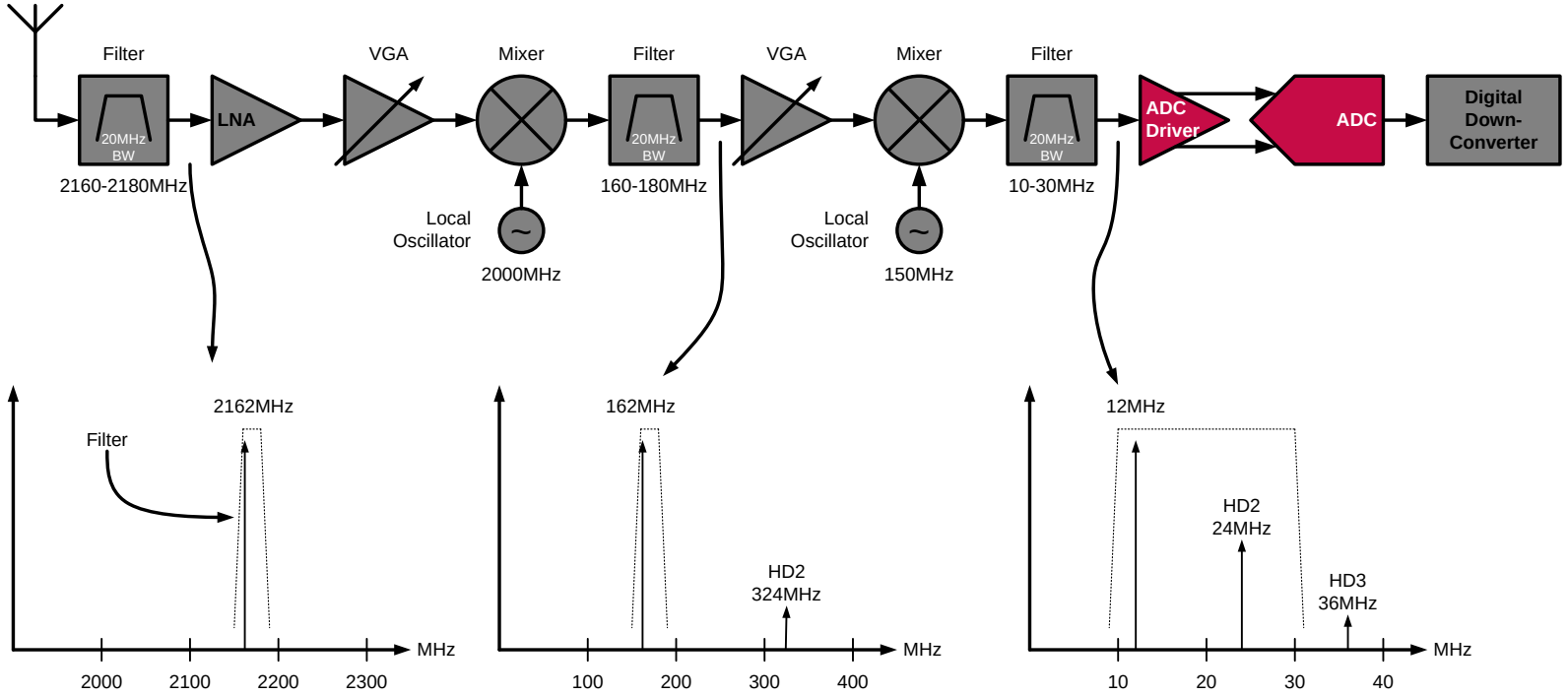


Mixer Example

ADC performance continues to increase but is still limited at very high frequencies. Mixers are used to translate signals to a lower frequency where they can be sampled.

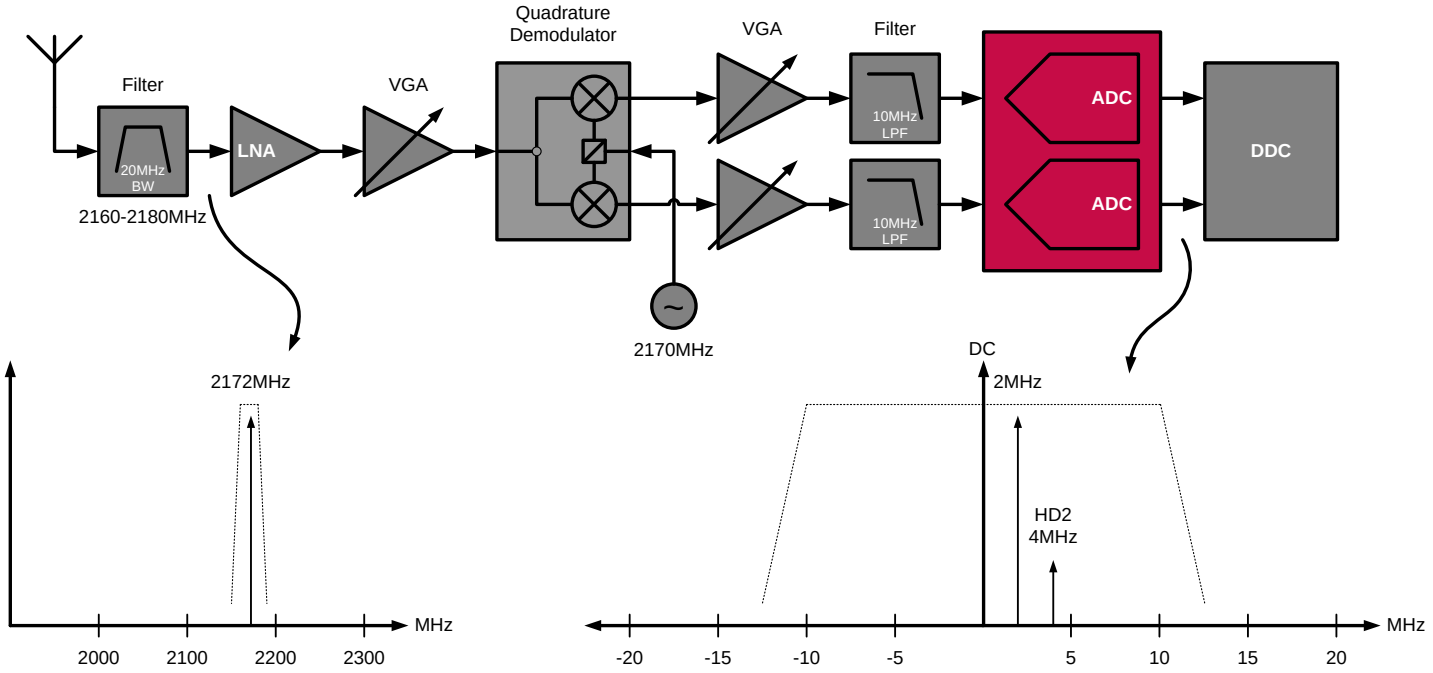


Low IF Superheterodyne Receiver



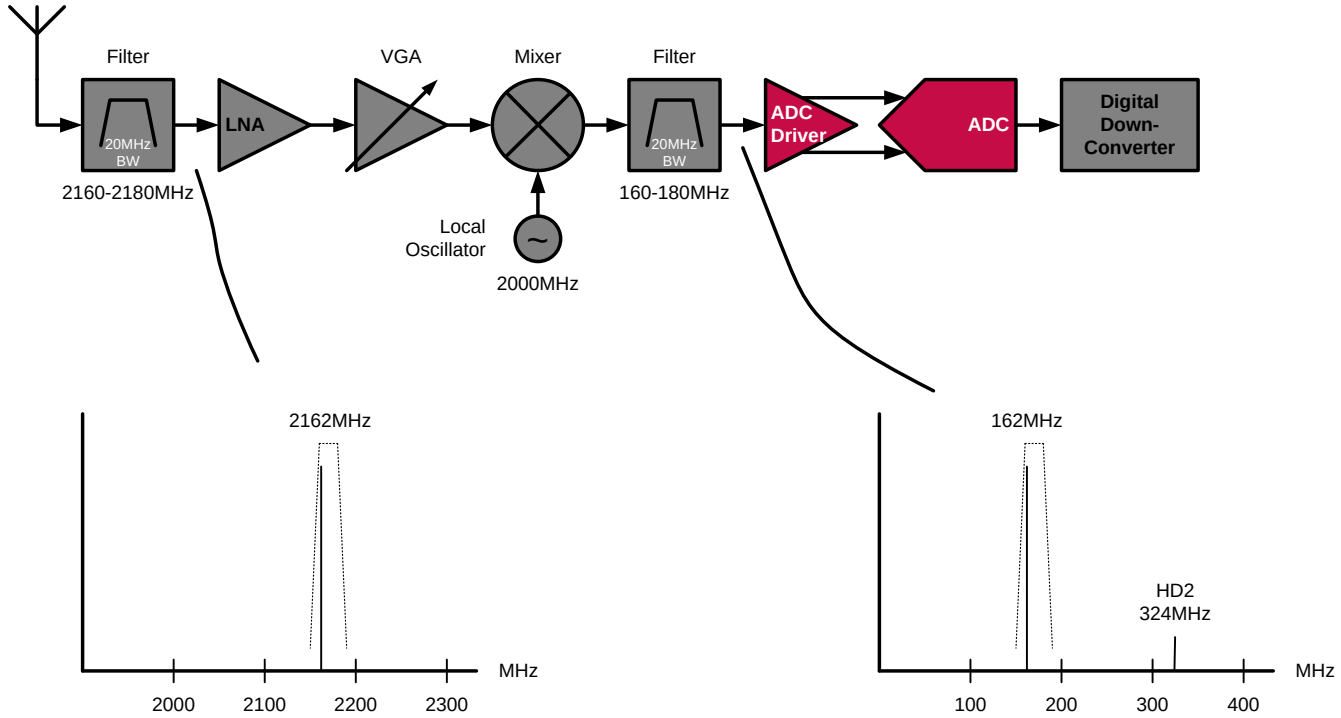
Architecture	Pros	Cons	ADC Requirements
Low-IF Superheterodyne	• Well Understood • Excellent Blocker Performance • Perfect I/Q Demodulation	• Higher BOM count/cost • Limited Flexibility • ADC Harmonics are In-Band	• Lower Speed • Moderate Performance

Zero-IF Receiver



Architecture	Pros	Cons	ADC Requirements
Direct Conversion Zero-IF (ZIF)	• Lowest Cost • Moderate ADC Requirements	• I/Q Impairments • ADC Harmonics are In-Band	• Dual Channel • Lower Speed • Moderate Performance

High-IF Receiver



Architecture	Pros	Cons	ADC Requirements
High-IF IF Sampling Sub-sampling	• Reduced Cost • Perfect I/Q Demodulation • ADC Harmonics are Out-of-Band	• Faster ADC • Higher Performance ADC	• High Input Bandwidth • Low Jitter • Good SNR/SFDR/IMD

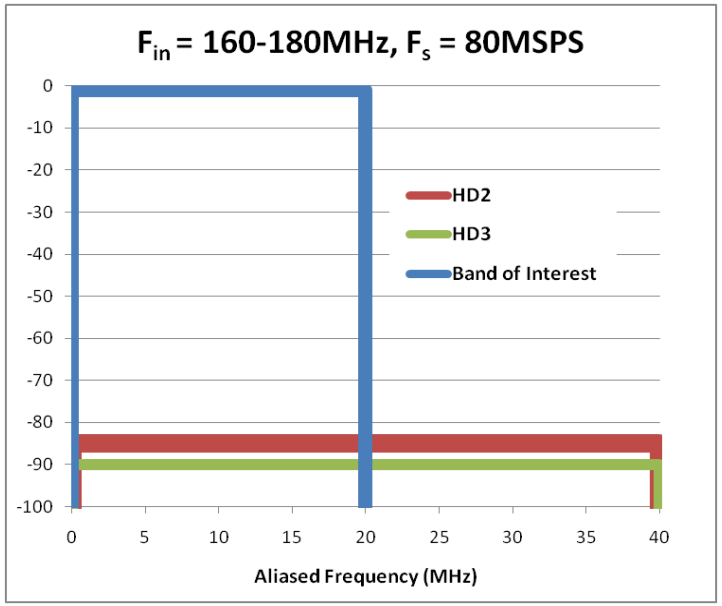
Higher Sample Rate Aids Frequency Planning

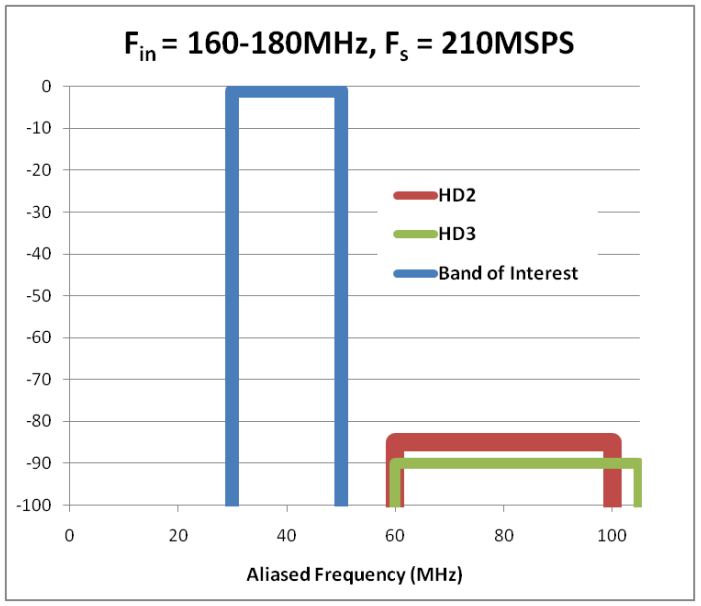
Avoid 2nd and 3rd harmonics to increase dynamic range

- Amplifier harmonics may be attenuated with filter but ADC harmonics can not
- Harmonics from either source may be avoided with careful frequency planning

Other Benefits of High Sample Rate

- More spectrum can be processed by a single ADC
- Doubling Fs gives 3dB more SNR in the desired channel
- Anti-aliasing filters are simplified





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ADC Specifications and SDR

Noise

- Limits the smallest signal that can be digitized

Linearity (Distortion)

- Distortion can mask desired signals

Resolution

- Sets quantization noise limiting ultimate sensitivity

Instantaneous Dynamic Range

- The maximum input level minus the noise and distortion
- Critical for multichannel wideband SDR receivers

ADC Specifications and SDR (cont'd)

Sample Rate

- High sample rate is closer to an ideal SDR
- High sample rate enables flexible frequency planning
- Can increase SNR in the desired channel
- Trade-off: sample rate vs. resolution

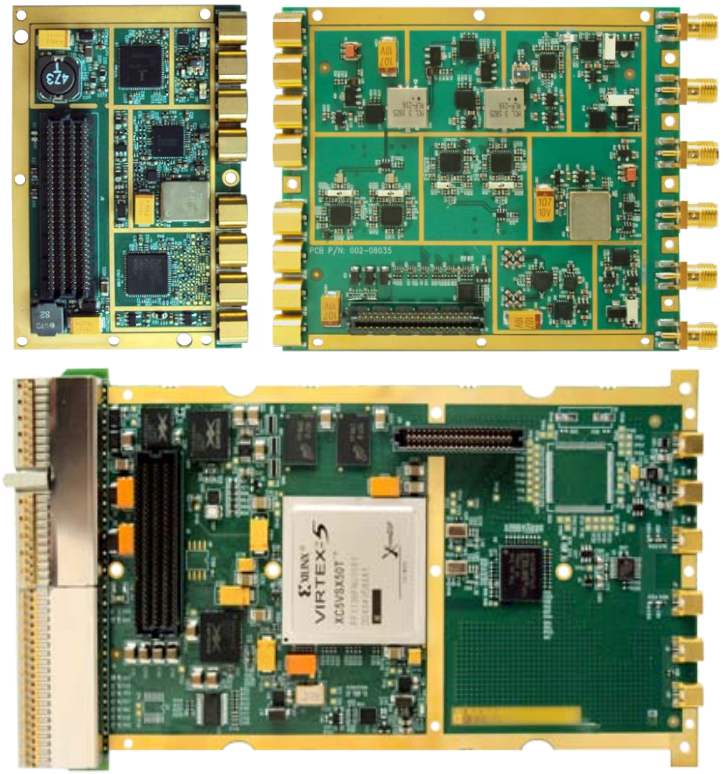
Power Consumption

- Affects battery life
- Affects reliability
- Limits the number of ADCs in high-density systems
- Trade-off: Dynamic range vs. sample rate vs. power consumption .

Design Considerations at System Level

Care and feeding of high-speed ADCs to ensure optimal performance:

- Sample clock purity
- Frequency Planning - Optimize IF frequency & bandwidth with sample rate
- High-quality analog filtering
- Analog and digital design practices
- Power supply
- Chassis



RF-4902 components:
Physical separation of analog and digital sections reduce interference

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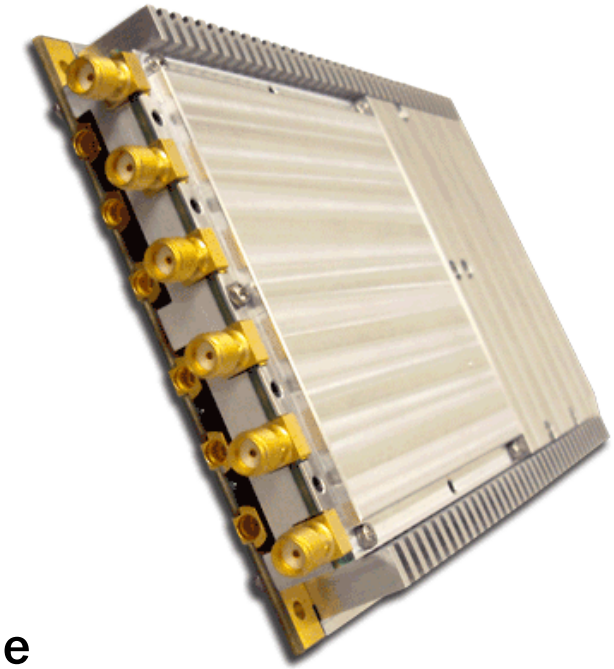
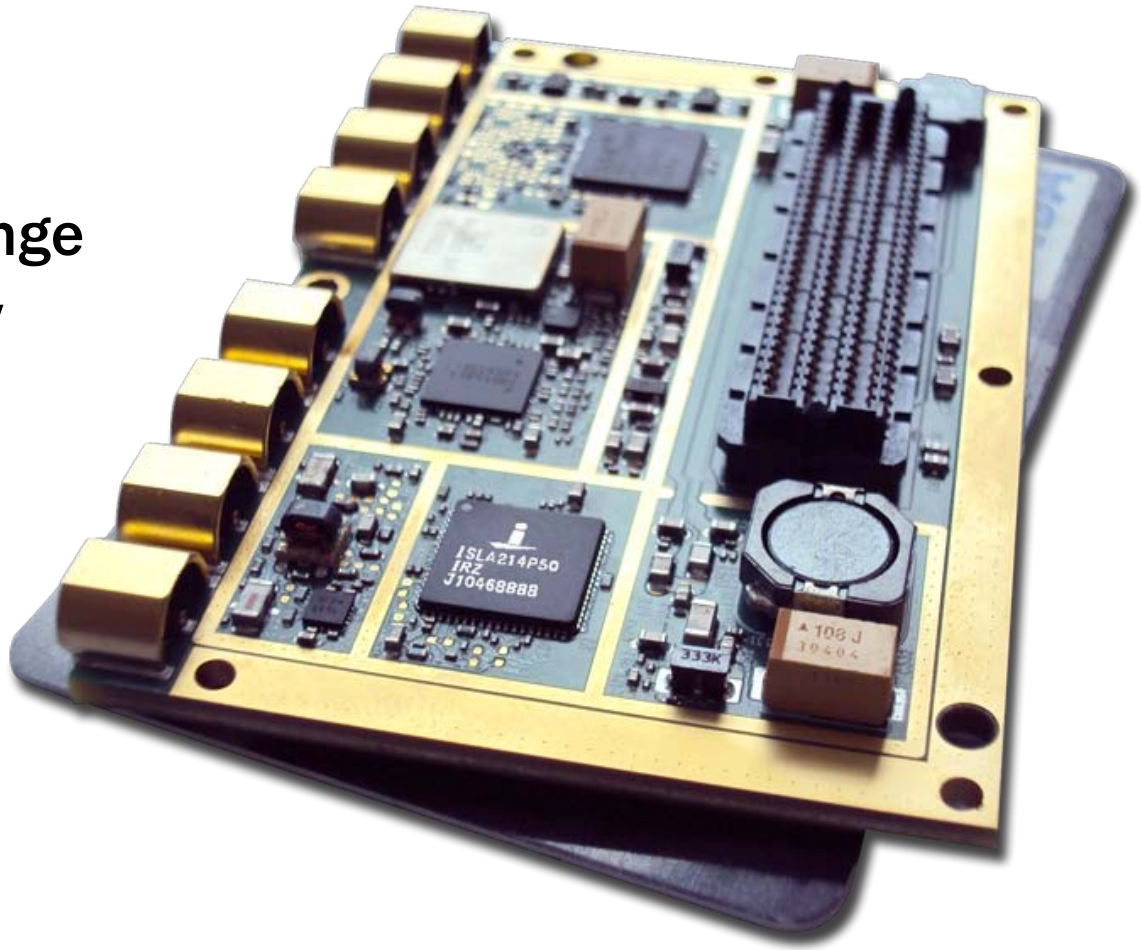
Spectrum's RF-4902 card

- Digitizes 195 MHz of bandwidth anywhere from 200 MHz to 2.7 GHz
- 14-bit ADC 490 MSPS
  - Intersil ISLA214P50
- 16-bit dual DAC 980 MSPS
  - Up to 400 MHz Transmitter analog bandwidth
- Xilinx Virtex-5 SX95T User FPGA for flexible IF signal processing
- Fast-frequency hopping up to 3000 hops/sec
- Integrated RF and Digital IF Processing in a single 3U cPCI slot

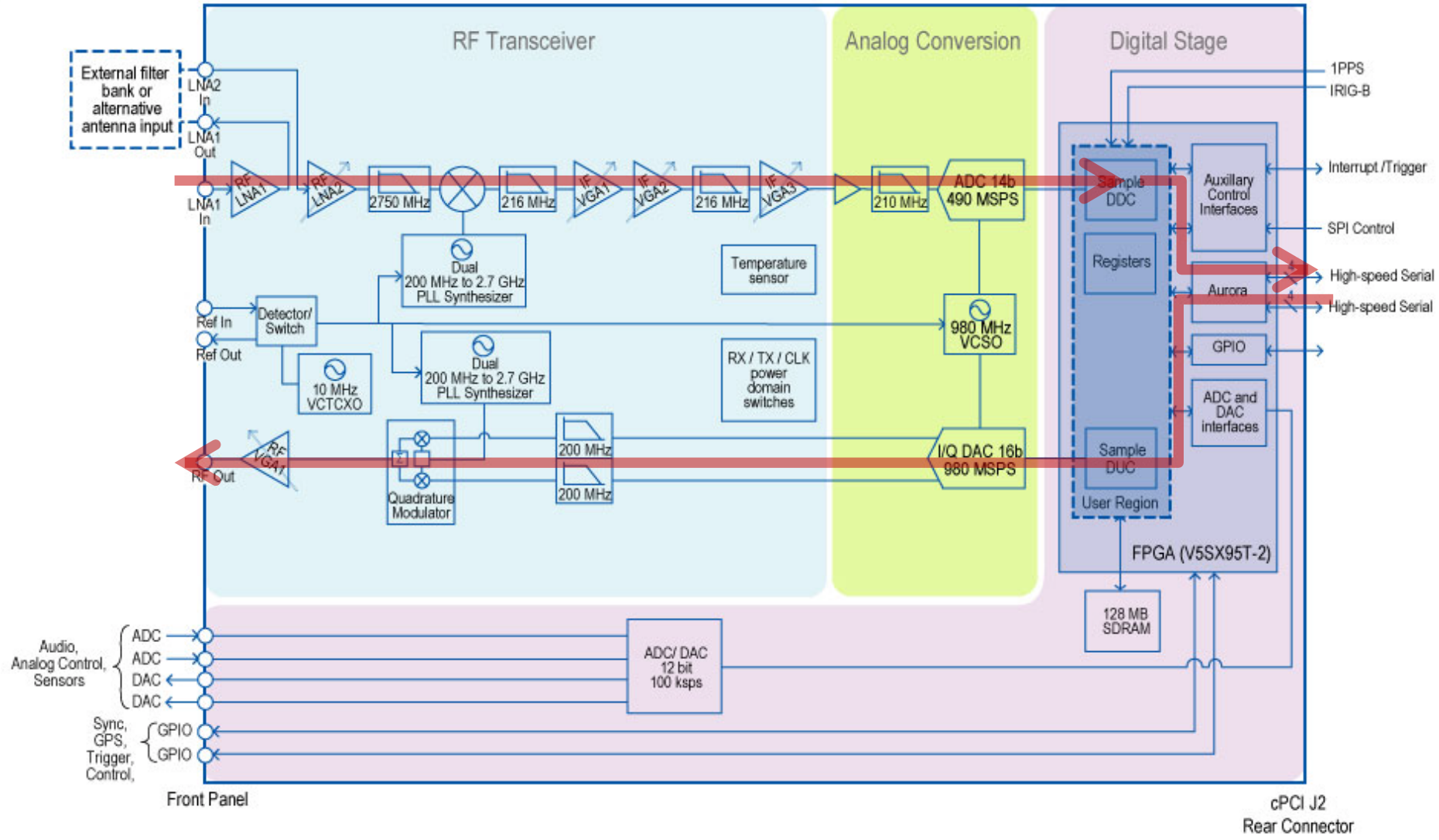


A Simplified Receiver Enables These Benefits

- Small footprint
- Low power
- High bandwidth
- High dynamic range
- Greater flexibility



RF-4902 Transceiver Block Diagram



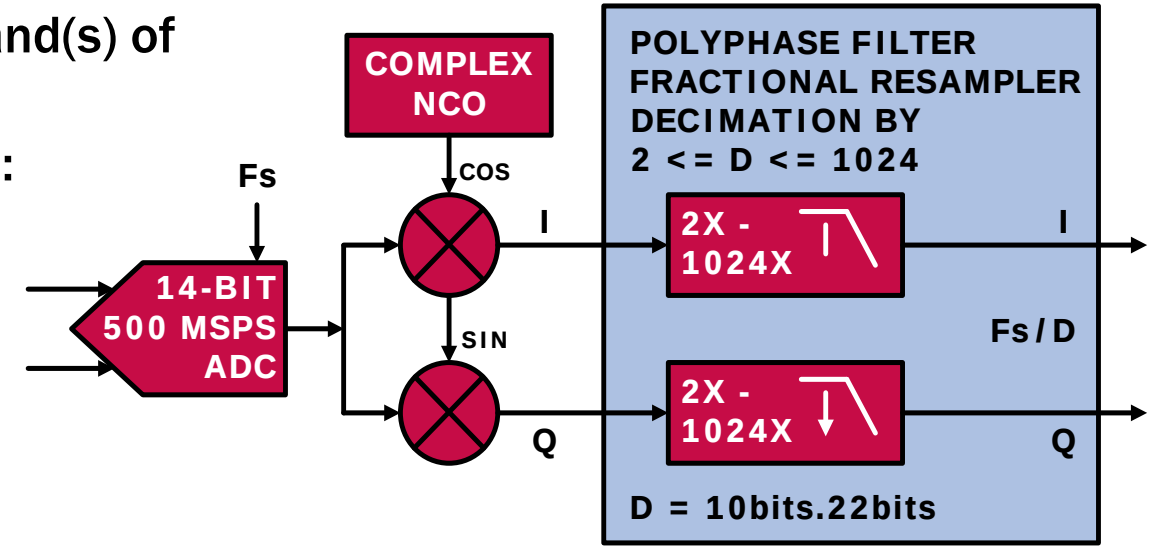
Digital Down Conversion

Digital Down Converter (DDC):

- Acts as second mixer stage of Superhet
- Performed digitally in FPGA
  - NCO replaces Local Oscillator
  - Multipliers replace mixer
- Desired frequency converted to baseband (0 Hz)
- Digital filter(s) to select band(s) of interest
- DDC's Advantages include:
  - Flexibility
  - Precision

DDC IP provided with the RF-4902:

- Dual phase to handle 490 MSPS ADC sampling rate
- Polyphase filter with fractional re-sampling
- Model-based design, using Simulink & Xilinx System Generator
- User configurable



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Many applications benefit from an SDR with these attributes

- wide instantaneous bandwidth
- high dynamic range
- small size, weight and power

High Speed, high-resolution ADCs help you get there

- Ability to simultaneously monitor more spectrum
- Higher sensitivity
- Adapt to different signal & waveform requirements
- Simplified frequency planning

Software Defined Radios are challenging

- Many conflicting requirements require good design trade-offs
- No single ideal design exists for all cases
- Proven platforms can reduce risk and speed system development

Contact Info

Thank You for Joining Us!

Spectrum Signal Processing
www.spectrumsignal.com

Tudor Davies
Director of Technology
(604) 676-6713

ADC.webinar@spectrumsignal.com

Intersil
www.intersil.com

Ed Kohler
Product Marketing Manager
(978) 805-6945

Mark Rives
Applications Engineer
(978) 805-6957

SDR.webinar@intersil.com

Questions?